

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor memory comprising:

a plurality of word lines, a plurality of bit lines and a plurality of memory cells, said plurality of memory cells each being connected to one of said plurality of word lines and one of said plurality of bit lines;

a Y decoder configured to drive said plurality of bit lines; and

a plurality of disconnecting devices, each provided between at least one corresponding bit line of said plurality of bit lines and said Y decoder, and being configured to (1) electrically disconnect said at least one corresponding bit line of said plurality of bit lines and said Y decoder, and (2) individually connect to a disconnection control circuit such that said plurality of disconnecting devices are independently controlled by said disconnection control circuit.

Claim 2 (Currently Amended): The semiconductor memory according to claim 1, wherein

said plurality of disconnecting device ~~includes~~ devices include a plurality of disconnecting devices, capable of electrically disconnecting those of said plurality of bit lines on which said plurality of disconnecting devices are provided integrally from said Y decoder.

Claim 3 (Currently Amended): The semiconductor memory according to claim 1, wherein

said plurality of disconnecting device ~~includes~~ devices include a plurality of disconnecting devices, capable of electrically disconnecting those of said plurality of bit lines

on which said plurality of disconnecting devices are provided individually from said Y decoder.

Claim 4 (Previously Presented): A semiconductor memory comprising:
a plurality of memory cells, each being connected to one of a plurality of word lines
and one of a plurality of bit lines;
a Y decoder configured to drive said plurality of bit lines;
a charge pump circuit connected to said Y decoder through a first switching circuit;
and
a port circuit configured to supply an external voltage to said Y decoder and
connected to said Y decoder through a second switching circuit.